

ECE-Sembrar

Website: www.rgcetpdy.ac.in



RAJIV GANDHI COLLEGE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE and Affiliated to Pondicherry University)

(Accredited with 'A' Grade by NAAC)

(Sponsored by Sri Balaji Educational and Charitable Public Trust)

Pondy - Cuddalore Main Road, Kirumampakkam, Puducherry - 607 403.

27.02.2019

From

P. Tamilselvan,
Assistant Professor (Stage II),
Department of ECE,
Rajiv Gandhi College of Engineering and Technology,
Kirumampakkam,
Puducherry - 607 403.

To

The Principal, Rajiv Gandhi College of Engineering and Technology, Kirumampakkam, Puducherry - 607 403.

THROUGH THE HEAD OF THE DEPARTMENT, DEPARTMENT OF ECE

Respected Sir,

Sub: - Request for permission to conduct a Two days workshop on "Recent Trends in VLSI Design" for IV Year ECE Students-reg.

We have planned to conduct a two day's workshop on the topic "Recent Trends in VLSI Design" on 01/03/2019 & 02/03/2019. I will be in-charge of the workshop. The aforementioned workshop will be offered to the IV Year / VIII Semester students of the ECE Department.

I kindly request you to grant permission to conduct this program. Enclosed are the details workshop for your perusal and approval.

of the workshop for your perusal and approval.

Thanking you

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B. & L

Yours sincerely,

P. Tamilselvan Event Incharge

Dr. E. VIJAYAKRISHNA RAPAKA

B.Tech. (Mech.), M.Tech.(Energy), Ph.D. (IIT Madras) M.I.S.T.E., F.I.I.P.E., M.C.S.I M.C.I.I.,

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

No: RGCET/ECE/Circular/2018-19/45

Date: 22.02.2019

CIRCULAR

We are excited to inform you that a two-day workshop on "Recent Trends in VLSI Design" from 01.03.2019 – 02.03.2019, is organized exclusively for our IV Year students This workshop is designed to provide both theoretical knowledge and practical skills essential for mastering these advanced VLSI Technologies.

Resource Person Details:

Mr.A.D.Senthilkumar, Senior Verification Engineer and

Mr.A.Robert Jean, Senior Design Engineer, Vistronics Design Solutions, Chennai

Venue: Seminar Hall

All are invited

HOD/ECE

Copy to:

1. The Principal

2. Circulate to all Faculty Members and ECE students

3. Notice board / file

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Dr. E. VIJAYAKRISHNA RAPAKA

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(NAAC ACCREDITED WITH GRADE A)

Pondy - Cuddalore Main Road, Kirumambakkam, Pondicherry - 607 403.

The HOD, Staff and Students of





C



Department cordially invite you to the inauguration of IETE Sponsored Two Days National Level Workshop on

"Recent Trends in VLSI Design"

On Friday, 1st March 2019 at 9.45 a.m in the Seminar Hall

Shri M. K. RAJAGOPALAN

Chairman

Sri Balaji Educational & Charitable Public Trust will preside over the function

Mr. A.D.SENTHILKUMAR

(Senior Verification Engineer) &

Mr. A.ROBERT JEAN

(Senior Design Engineer) Vistronics Design Solutions Chennai

will be the Chief Guests and address the gathering

Dr. E. VIJAYAKRISHNA RAPAKA

Principal, RGCET will felicitate

Dr. K. AYYAPPAN

Vice-Principal, RGCET will honor

Mrs. B. SHOBA HOD, ECE

will welcome the gathering

N

M.I.S.T.E., F.I.I.P.E., M.C.S.I M.C.I.I.,

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Pondy - Cuddalore Main Road.

TE STUDENTS FORUM (ISF)



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Report: Workshop on Recent Trends in VLSI Design

Name of the Department	Department of Electronics and Communication
Name of the Event Organized	Workshop on Recent Trends in VLSI Design
Date of the Event Organized	01/03/2019 & 02/03/2019
Time	9.00 am – 4.00 pm
No. of participants	63
Name of the Chief Guest / Speakers	Mr.A.D.Senthilkumar ,Senior Verification Engineer and Mr.A.Robert Jean, Senior Design Engineer, Vistronics Design Solutions, Chennai
Venue	Seminar Hall, Administrative Block

Seminar Objectives:

- 1. Provide participants with an understanding of advanced VLSI design concepts and techniques.
- 2. Explore emerging trends such as low-power design, hardware security, and neuromorphic computing.
- 3. Foster hands-on learning through practical exercises or case studies.
- 4. Facilitate networking and knowledge sharing among participants and industry experts.

Seminar Schedule:

Date	Time	Topics covered	
	9.30 am – 11.30 am	Fundamentals and Advanced Techniques – Introduction to VLSI Design	
	11.30 am - 11.45am	Tea Break	
01/03/19	11.45 am - 1.00 pm	Advanced CMoS Technologies	
01/03/19	1.00 pm - 1.45 pm	Lunch Break	
	1.45 pm – 2.45 pm	Low power Design Techniques	
	2.45 pm – 3.00 pm	Tea Break	
	3.00 pm – 4.00 pm	High Speed Design and Signal Integrity	
	9.30 am – 11.30 am	Emerging Trends and Practical Applications – Hardware Security	
	11.30 am - 11.45am	Tea Break	
02/03/19	11.45 am - 1.00 pm	Neuromorphic Computing	
02/03/19	1.00 pm – 1.45 pm	Lunch Break	
	1.45 pm – 2.45 pm	Quantum Computing and VLSI	
	2.45 pm – 3.00 pm	Tea Break	
	3.00 pm – 4.00 pm	Case Studies	



Dr. E. VIJAYAKRISHNA RAPAKA
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The two-day workshop conducted on the topic "Recent Trends in VLSI Design", was held on March 01/03/2019& 02/03/2019. The speakers for the workshopwere invited from industry Vistronics Design Solutions, Chennai. The workshop was aimed at providing ECE students with basic essential knowledge like essentials of Verilog HDL Programming Concepts, covering both basic and advanced functionalities and to equip them with practical skills for VLSI applications. Moreover,industrial simulation tools that are used for design and development of real time projects was also discussed as case study. The workshop was designed to cover various aspects of Digital Concepts, from understanding different types modeling concepts in Verilog HDL.

The target participant for the workshop was Final Year ECE department students. A total of 63

students attended the workshop.

EventIncharge

Mr. P. Tamilselvan

Assistant Professor(Stage II),

Department of ECE

Rajiv Gandhi College of Engineering and Technology

Date:02/03/2019

Head of the Department

HEAD OF THE DEPARTMENT Electronics and Convertication Engo Stir Canalists and A lect



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List of Students Attended

Academic Year: 2018-19

Name of the Program: Recent Trends in VLSI Design

S.No	Register Number	Name	Year /Sem	Department	
1	14TC0407	ALAM HUSSAIN	IV/VIII	ECE	
2	15TC0501	AISWARYA M	IV/VIII	ECE	
3	15TC0503	AMANULLAH N	IV/VIII	ECE	
4	15TC0504	AMRUTHA P	IV/VIII	ECE	
5	15TC0505 ANAGA MALINI S		IV/VIII	ECE	
6	15TC0506	ANBARASAN K	IV/VIII	ECE	
7	15TC0507	ARTHI H	IV/VIII	ECE	
8	15TC0508	ARUN RATHNARAJ P	IV/VIII	ECE	
9	15TC0509	BABY ANILAA R	IV/VIII	ECE	
10	15TC0510	BOOPITHA V	IV/VIII	ECE	
11	15TC0511	DHANAPRIYA K	IV/VIII	ECE	
12	15TC0512	DIVYA J	IV/VIII	ECE	
13	15TC0513	GAYATHRI V	IV/VIII	ECE	
14	15TC0514	GIRIDHARAN R	IV/VIII	ECE	
15	15TC0515	GURU ARAVINDHAN S	IV/VIII	ECE	
16	15TC0516	HARISH KUMAR M	IV/VIII	ECE	
17	15TC0517	HEMAPRIYA K	IV/VIII	ECE	
18	15TC0518	JENCY SAGAYARANI A	IV/VIII	ECE	
19	15TC0519	JEYASEELAN K	IV/VIII	ECE	

Dr. E. Valla III. San Alfa B.Tech. (Mech., Alleman San Asias) W. B. Carriera, M. S. M.C.I.I., FRINCIPAL





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S.No	Register Number	Name	Year /Sem	Department
20	15TC0520	KABILAN P	IV/VIII	ECE
21	15TC0521	KALPANA J	IV/VIII	ECE
22	15TC0522	KARTHIK R	IV/VIII	ECE
23	15TC0523	KARTHIKA R	IV/VIII	ECE
24	15TC0524	KARTHIKEYAN S	IV/VIII	ECE
25	15TC0525	MANIMEGALAI N	IV/VIII	ECE
26	15TC0526	MANIKANDAN D	IV/VIII	ECE
27	15TC0527	MANIKANDAN N	IV/VIII	ECE
28	15TC0528	MARTINA AGNES DEVAKIRUBAI T	IV/VIII	ECE
29	15TC0530	MOHAMMED AZARUDEEN J	IV/VIII	ECE
30	15TC0531	MOHANRAJ V	IV/VIII	ECE
31	15TC0533	NIRMAL KUMAR R	IV/VIII	ECE
32	15TC0535	PARTHIBAN R	IV/VIII	ECE
33	15TC0536	PAVITHRA K	IV/VIII	ECE
34	15TC0538	PRADHEEP S	IV/VIII	ECE
35	15TC0539		IV/VIII	ECE
36	15TC0540	PREETHI M	IV/VIII	ECE
37	15TC0541	PREETHI R	IV/VIII	ECE
38	15TC0543	PRIYADHARSHINI J	IV/VIII	ECE

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S.No	Register Number	Name	Year /Sem	Department
39	15TC0544	PRIYANKA L	IV/VIII	ECE
40	15TC0545	PRIYANKA. V	IV/VIII	ECE
41	15TC0547	RAJESHWARI S	IV/VIII	ECE
42	15TC0548	RASHMI R	IV/VIII	ECE
43	15TC0549	RATHINAMURUGAN D	IV/VIII	ECE
44	15TC0550	RAVICHANDRAN N	IV/VIII	ECE
45	15TC0551	REGINA D	IV/VIII	ECE
46	15TC0553	SAKTHI BALAJI P	IV/VIII	ECE
47	15TC0554	SANMUGA PRIYA M	IV/VIII	ECE
48	15TC0555	SANTHA KUMAR R S	IV/VIII	ECE
49	15TC0556	SASIREKHA P	IV/VIII	ECE
50	15TC0557	SOUMYA TAZE R	IV/VIII	ECE
51	15TC0558	SOWMIYA S	IV/VIII	ECE
52	15TC0560	SRUDHI R	IV/VIII	ECE
53	15TC0562	SUSHMITHAA S	IV/VIII	ECE
54	15TC0564	THIRUSELVAM K	IV/VIII	ECE
55	15TC0565	THIRUVARASAN S	IV/VIII	ECE
56	15TC0566	UDAYAKUMAR R	IV/VIII	ECE
57	15TC0567	VAITHEESHWARAN I	IV/VIII	ECE

Dr. E. VIJAVARTINIKIA RAPAKA B.Tech. (Mech.): M.Tech. (Energy), Ph.D. (IIT Madras) M.J.S.T.E., FILPLE, M.C.S.I.M.C.I.I., PRINCIPAL





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S.No	Register Number	Name	Year /Sem	Department
58	15TC0568	VASANTHVELAN J	IV/VIII	ECE
59	15TC0569	VENKATESH A	IV/VIII	ECE
60	15TC0570	VENKATESH S	IV/VIII	ECE
61	15TC0571	VIJAYABHARATHI K IV/VIII		ECE
62	15TC0572	YUDHASITH R	IV/VIII	ECE
63	15TC0573	YUVASRI S	IV/VIII	ECE
Total E	nrolled Stud	ents		63

Event Incharge

Head of the Department

HEAD OF THE DEPARTMENT

Electronics And Communication Engg Rajiv Gandhi College of Engg. & Tech PUDUCHERRY - 607 402



Dr. E. VIJAYARRISHNA RAPAKA B.Tech. (Mech.), M.Tech. (Energy), Ph.D. (IIT Madras) M.I.S.T.E., F.I.I.P.E., M.C.S.I M.C.I.I., PRINCIPAL



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Attendance Sheet

Year / Semester: IV/VIII

Academic Year: 2018-19

Name of the Program: Recent Trends in VLSI Design

S.No	Register Number	Name	01/03/2019	02/03/2019
1	14TC0407	ALAM HUSSAIN	P	A
2	15TC0501	AISWARYA M	A	7
3	15TC0503	AMANULLAH N	P !	P
4	15TC0504	AMRUTHA P	P	P
5	15TC0505	ANAGA MALINI S	P	P
6	15TC0506	ANBARASAN K	P	P
7	15TC0507	ARTHI H	P	P
8	15TC0508	ARUN RATHNARAJ P	P	P
9	15TC0509	BABY ANILAA R	P	P
10	15TC0510	BOOPITHA V	P	P
11	15TC0511	DHANAPRIYA K	P	P
12	15TC0512	DIVYA J	P	7
13	15TC0513	GAYATHRI V	P	P
14	15TC0514	GIRIDHARAN R	P	P
15	15TC0515	GURU ARAVINDHAN S	P	P
16	15TC0516	HARISH KUMAR M	A	7
17	15TC0517	HEMAPRIYA K	P	7
18	15TC0518	JENCY SAGAYARANI A	7	P
19	15TC0519	JEYASEELAN K	A-	P
20	15TC0520	KABILAN P	7	P
21	15TC0521	KALPANA J	7	P
22	15TC0522	KARTHIK R	17	P
23	15TC0523	KARTHIKA R	7	A

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S.No	Register Number	Name	01/03/2019	02/03/2019
24	15TC0524	KARTHIKEYAN S	P	P
25	15TC0525	MANIMEGALAI N	P	P
26	15TC0526	MANIKANDAN D	P	P
27	15TC0527	MANIKANDAN N	P	P
28	15TC0528	MARTINA AGNES DEVAKIRUBAI T	P	P
29	15TC0530	MOHAMMED AZARUDEEN J	P	P
30	15TC0531	MOHANRAJ V	A	P
31	15TC0533	NIRMAL KUMAR R	P	P
32	15TC0535	PARTHIBAN R	P	P
33	15TC0536	PAVITHRA K	P	P
34	15TC0538	PRADHEEP S	P	P
35	15TC0539	PREETHA P	P	P
36	15TC0540	PREETHI M	A	P
37	15TC0541	PREETHI R	P	P
38	15TC0543	PRIYADHARSHINI J	P	7
39	15TC0544	PRIYANKA L	P	P
40	15TC0545	PRIYANKA. V	P	Á
41	15TC0547	RAJESHWARI S	P	7
42	15TC0548	RASHMI R	P	P
43	15TC0549	RATHINAMURUGAN D	P	7
44	15TC0550	RAVICHANDRAN N	P	A
45	15TC0551	REGINA D	P	7
46	15TC0553	SAКТНІ ВАLАЛ Р	P	A
47	15TC0554	SANMUGA PRIYA M	P	P

dr. E. VIJAVAKRISHNA RAPAKA

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M.I.S.T.E., F.I.I.P.E., M.C.S.I M.C.I.I.,

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S.No	Register Number	Name	01/03/2019	02/03/2019
48	15TC0555	SANTHA KUMAR R S	P	7
49	15TC0556	SASIREKHA P	P	P
50	15TC0557	SOUMYA TAZE R		P
51	15TC0558	SOWMIYA S	P	P
52	15TC0560	SRUDHI R	P	P
53	15TC0562	SUSHMITHAA S	P	P
54	15TC0564	THIRUSELVAM K	P	P
55	15TC0565	THIRUVARASAN S	P	P
56	15TC0566	UDAYAKUMAR R	P	P
57	15TC0567	VAITHEESHWARAN I	P	P
58	15TC0568 VASANTHVELAN J		P	P
59	15TC0569	VENKATESH A	P	P
60	15TC0570	VENKATESH S	P	P
61	15TC0571	VIJAYABHARATHI K	P	P
62	15TC0572	YUDHASITH R	A	P
63	15TC0573	YUVASRI S	P	P
Total N	umber of Stud	dents	63	63
Total St	tudents Absen	t	3	2
Γotal St	udents Presen	t	60	61

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Workshop Photos:







IETE Sponsored two days National level workshop on Recent Trends in VLSI Design with the Chief Guests Mr.A.D.Senthilkumar and Mr.A.Robert Jean from Vistronics Design Solutions,

Chennai



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<u>FEE1</u>	DBACK FORM					
Work	ship Tittle					
Date:			Venu	ıe:		
Name	·					
Regist	ter Number:	Seme	ester/Year:			
	DESIGN OF THE CO					
A.	Were objectives of t	he workshop (clear to you?	Y /N		
В.	The workshop conte	ents met with y	our expectat	ions		
	1. Strongly disagree	2. Disagree	3. Neutral	4. Agree	5. Strongly agree	
C.	The lecture sequence	e was well plan	nned	Ü	0,70	
	1. Strongly disagree			4. Agree	5. Strongly agree	
D.	The contents were il		adequate exa	amples		
	1. Strongly disagree		3. Neutral	4. Agree	5. Strongly agree	
E.	The level of the worl					
- 1	1. Strongly disagree		3. Neutral		5. Strongly agree	
F.	The workshop conte	nts compared	with your ex			
~	1. Strongly disagree		3. Neutral	4. Agree	5. Strongly agree	
G.	The workshop expos	ed you to new				
	1. Strongly disagree	2. Disagree	3. Neutral	4. Agree	5. Strongly agree	
THE C	CONDUCT OF THE	COURSE				
	TTL . I					
A.	The lectures were cle	ear and easy to		9 90000		
D	1. Strongly disagree		3. Neutral	4. Agree	5. Strongly agree	
В.	The teaching aids we			4		
0	1. Strongly disagree	2. Disagree	3. Neutral	4. Agree	5. Strongly agree	
C.	The workshop mater 1. Strongly disagree	Tai nanded ou			5 C. 1	
n	The instructors once	2. Disagree	3. Neutral	4. Agree	5. Strongly agree	
D.	The instructors enco	2 Discourse	2 Nantual		5 Ct 1	
F	1. Strongly disagree Were objectives of the	2. Disagree	3. Neutral	4. Agree	5. Strongly agree	
E.	Please give overall ra	ting of the su	zeu: I / IN			
Γ.	I lease give overall ra	iting of the wo	rksnop			
	90% - 100% () 60% - 7	70% ()			
	80% - 90% (50% - 6	60% ()			
	70% - 80% (below :	50% ()	Signatu	re	
					(10)	E

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Multiple Choice Questions:	
Multiple Choice Questions.	d) system on a circuit
	7. Which is the high level representation of
Name:	VLSI design?
	a) problem statement
Department/Sec:	b) logic design
	c) HDL program
Workshop Title:	d) functional design
	8 is used in logic design of VLSI.
1. VLSI technology uses to form	a) LIFO
integrated circuit.	b) FIFO
a) transistors	c) FILO
b) switches	d) LILO
c) diodes d) buffers	
2. Madium goals integration has	9. Which provides higher integration density?
2. Medium scale integration has	a) switch transistor logic
a) ten logic gates	b) transistor buffer logic
b) fifty logic gatesc) hundred logic gates	c) transistor transistor logic
d) thousands logic gates	d) circuit level logic
d) mousands logic gates	
3. The difficulty in achieving high doping	10. Physical and electrical specification is given
concentration leads to	in
a) error in concentration	a) architectural design
b) error in variation	b) logic design c) system design
c) error in doping	d) functional design
d) distribution error	d) functional design
4 is used to deal with effect of	
variation.	
a) chip level technique	
b) logic level technique	
c) switch level technique	
d) system level technique	
5. As die size shrinks, the complexity of	E OF ENGINEERIN
making the photomasks	Sign Control of the second
a) increases	Topartment Execution
b) decreases	(1) \(\begin{align*} \lambda \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\
c) remains the same	
d) cannot be determined	-vaucher -
6 architecture is used to design VLSI.	
a) system on a device b) single open circuit	
c) system on a chip	Dr. E. VIJAYAKRISHNA RAPAKA
c) system on a cmp	B.Tech. (Mech.), M.Tech.(Energy), Ph.D. (IIT Madras) M.I.S.T.E., F.I.I.P.E., M.C.S.I M.C.I.I., PRINCIPAL
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RAJIV GANDHI COLLEGE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE and Affiliated to Pondicherry University)

(Accredited with 'A' Grade by NAAC)

(Sponsored by Sri Balaji Educational and Charitable Public Trust)

Pondy - Cuddalore Main Road, Kirumampakkam, Puducherry - 607 403.

Signature

Answers:

1.a

2.c

3.b

4.d

5. a

6. c

7. a

8. b

9.c 10.d



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FEEDRACK FORM

LULU	Direct I Oldin					
Works	hip Tittle Recen	t Trenol	s. ™ .√S	LI De	zigh,	
Date: .	2/3/2019		Ver	iue: Seni	nay Hall.	•
Name:	Sushmithac	n. S				
Regist	er Number: !5.TCO!	5.62Sem	ester/Year:	4.44/8.5	zm,	
THE I	DESIGN OF THE C	OURSE				
A.	Were objectives of t	he workshop	clear to you?	YIN		
В.	The workshop cont	ents met with	your expecta	itions		
	1. Strongly disagree				5. Strongly agree	
C.	The lecture sequence	e was well pla	nned			
	1. Strongly disagree	2. Disagree	3. Neutral	4. Agree	5. Strongly agree	
D.	The contents were i	llustrated with	adequate ex	xamples		
	1. Strongly disagree				-5. Strongly agree	
E.	The level of the wor	kshop was too	high			
	1. Strongly disagree	2. Disagree	3. Neutral	4. Agree	5. Strongly agree	
F.	The workshop cont	ents compared	with your e	xpectations wa	s too theoretical	
	1. Strongly disagree				5. Strongly agree	
G.	The workshop expo	sed you to nev	v knowledge	and practices		
	1. Strongly disagree				5. Strongly agree	
THE (CONDUCT OF THE	COURSE				

A. The lectures were clear and easy to understand 1. Strongly disagree 2. Disagree 4. Agree 5. Strongly agree 3. Neutral B. The teaching aids were effectively used 1. Strongly disagree 2. Disagree 3. Neutral 5. Strongly agree 4. Agree C. The workshop material handed out was adequate 5. Strongly agree 1. Strongly disagree 2. Disagree 3. Neutral 4. Agree D. The instructors encouraged interaction and were helpful 1. Strongly disagree 2. Disagree 3. Neutral A. Agree 5. Strongly agree E. Were objectives of the course realized? X/N F. Please give overall rating of the workshop

> 90% - 100% () 60% - 70% 80% - 90% () 50% - 60% () 70% - 80% () below 50% ()



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FEEDBACK	FORM
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Works	hip TittleRecent	- terends	in VL	ST Des	เ๊ลูก
Date: .	02/03/201	9	Venue	eSemi	nar Hall
Name:	Hema nuiga	· K			
Regist	er Number:15.T.C	0.5.1.7Seme	ester/Year:	Dy Vinta	Sem
	DESIGN OF THE CO				
A.	Were objectives of the	he workshop o	lear to you?	Y/N	
B.	The workshop conte	ents met with y	our expectation	ons	
	1. Strongly disagree	2. Disagree	3. Neutral	4. Agree	5. Strongly agree
C.	The lecture sequenc		nned		
	1. Strongly disagree		3. Neutral	4. Agree	5. Strongly agree
D.	D. The contents were illustrated with adequate examples				
	1. Strongly disagree		3: Neutral	4. Agree	5. Strongly agree
E.	The level of the worl		high	C	
	1. Strongly disagree		3 Neutral	4. Agree	5. Strongly agree
F.	F. The workshop contents compared with your expectations was too theoretical				
2.	1. Strongly disagree		3. Neutral	4. Agree	5. Strongly agree
G.	The workshop expos			0	
٥.	1. Strongly disagree		3. Neutral	4. Agree	5. Strongly agree
THE (CONDUCT OF THE	COURSE			

A.	The lectures were cl	ear and easy	o understand		
	1. Strongly disagree	2. Disagree	3. Neutral	4. Agree	5. Strongly agree
B.	The teaching aids w	ere effectively	used		
	1. Strongly disagree	2. Disagree	3. Neutral	4. Agree	5. Strongly agree
C.	C. The workshop material handed out was adequate				
	1. Strongly disagree	2. Disagree	3. Neutral	4. Agree	5. Strongly agree
D.	D. The instructors encouraged interaction and were helpful				
	1. Strongly disagree	2. Disagree	3. Neutral	4. Agree	5. Strongly agree
E.	. Were objectives of the course realized? Y/N				
F.	Please give overall r	ating of the w	orkshop		

90% - 100% (*) 60% - 70% () 50% - 60% () 80% - 90% () flema p Signature 70% - 80% () below 50% ()

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> PRINCIPAL



FEEDBACK FORM

reeu	DBACK FURIN			
	ship Tittle. Recent trand in 1921. Design			
Date: .		ue: <i>Bl.min</i>	29 hall	••
Name:	E nobyet-nodok :=			
Regist	ster Number: .\5.TC.0568Semester/Year:			
THE I	DESIGN OF THE COURSE			
В.	. Were objectives of the workshop clear to you? The workshop contents met with your expectation. Strongly disagree 2. Disagree 3. Neutral	×/N tions 4. Agree	5. Strongly agree	
	 The lecture sequence was well planned 1. Strongly disagree 2. Disagree 3. Neutral The contents were illustrated with adequate ex 	A. Agree	5. Strongly agree	
	1. Strongly disagree 2. Disagree 3. Neutral The level of the workshop was too high	4. Agree	5. Strongly agree	
	1. Strongly disagree 2. Disagree 3. Neutral The workshop contents compared with your example 1. Strongly disagree 2. Disagree 3. Neutral	4. Agree expectations w 4. Agree	5. Strongly agree as too theoretical 5. Strongly agree	
G.	The workshop exposed you to new knowledge 1. Strongly disagree 2. Disagree 3. Neutral			
THE C	CONDUCT OF THE COURSE			
	The lectures were clear and easy to understand 1. Strongly disagree 2. Disagree 3. Neutral	l 4. Agree	S. Strongly agree	
	The teaching aids were effectively used 1. Strongly disagree 2. Disagree 3. Neutral	4. Agree	5. Strongly agree	
C.	The workshop material handed out was adequal. Strongly disagree 2. Disagree 3. Neutral	ate A. Agree	5. Strongly agree	
	The instructors encouraged interaction and we 1. Strongly disagree 2. Disagree 3. Neutral		5. Strongly agree	
	Were objectives of the course realized? \mathcal{A}/N Please give overall rating of the workshop	777		

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Multiple Choice Questions:	
Surala °LD G	7. Which is the high level representation of
Name: Sushmitahaa-S.	VLSI design?
15TC0562	a) problem statement
Department/Sec: ECE.	b) logic design
1.55	c) HDL program
Workshop Title: Recent Trends in VSLI Design	d) functional design
VSLI Design	
	8 is used in logic design of VLSI.
1. VLSI technology uses to form	a) LIFO
integrated circuit.	b) FIFO
a) transistors	c) FILO
b) switches c) diodes	d) LILO
d) buffers	
d) buriers	0.3371.1
2. Medium scale integration has	9. Which provides higher integration density?
a) ten logic gates	a) switch transistor logic
b) fifty logic gates	b) transistor buffer logic
c) hundred logic gates	c) transistor transistor logic
d) thousands logic gates	d) circuit level logic
	10. Physical and electrical specification is given
3. The difficulty in achieving high doping	in
concentration leads to	a) architectural design
a) error in concentration	b) logic design
b) error in variation	c) system design
c) error in doping	d) functional design
d) distribution error	
4 is used to deal with effect of	# A.
variation.	\$a
a) chip level techniqueb) logic level technique	
c) switch level technique	Cilipae
d) system level technique	Na van
5. As die size shrinks, the complexity of	Signature
making the photomasks	
a) increases	
b) decreases	
c) remains the same	SOLOF ENGINEER
d) cannot be determined	
6 architecture is used to design VLSI.	(E) (vopulment) E
a) system on a device	Wal for Jal
b) single open circuit	Carried States
e) system on a chip	aliche (
d) system on a circuit	

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Multiple Choice Questions:	
	7. Which is the high level representation of
Name: Hema pulya·K	VLSI design?
15tc0517	æ problem statement
Department/Sec: £CE	b) logic design
LCL	c) HDL program
Workshop Title:	d) functional design
	8 is used in logic design of VLSI.
1. VLSI technology uses to form	a) LIFO
integrated circuit.	b) FIFO
a) transistors	c) FILO
b) switches	d) LILO
c) diodes	
d) buffers	
	9. Which provides higher integration density?
2. Medium scale integration has	a) switch transistor logic
a) ten logic gates	b) transistor buffer logic
b) fifty logic gates	e) transistor transistor logic
c) hundred logic gates	d) circuit level logic
d) thousands logic gates	a) enemi ie ie ie gie
	10. Physical and electrical specification is given
3. The difficulty in achieving high doping	in
concentration leads to	a) architectural design
a) error in concentration	b) logic design
b) error in variation	c) system design
c) error in doping	d) functional design
d) distribution error	
4 is used to deal with effect of	
variation.	
a) chip level technique	
b) logic level technique	
c) switch level technique	Hema miyo Signature
d) system level technique	Signature
5. As die size shrinks, the complexity of	
making the photomasks	
a) increases	
b) decreases	EST OF ENGINEES
c) remains the same	31
d) cannot be determined	Department (S)
6 architecture is used to design VLSI.	113\ exe /8//
a) system on a device	May Louis A. S.
b) single open circuit	"Gaucher"
c) system on a chip	
d) system on a circuit	2

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Multiple Choice Questions:	
Name:-Yasanthrelan 5 (15700568)	7. Which is the high level representation of VLSI design?
	a) problem statement
Department/Sec: ECE	b) logic design
	c) HDL program
Workshop Title: Recent trends in VISI Design	d) functional design
1 XXX CX . 1 . 1	8 is used in logic design of VLSI.
1. VLSI technology uses to form	a) LIFO
integrated circuit.	b) FIFO
a) transistors	c) FILO
b) switches	d) LILO
c) diodes	
d) buffers	
	9. Which provides higher integration density?
2. Medium scale integration has	a) switch transistor logic
a) ten logic gates	b) transistor buffer logic
b) fifty logic gates	e) transistor transistor logic
e) hundred logic gates	d) circuit level logic
d) thousands logic gates	
3. The difficulty in achieving high doping	10. Physical and electrical specification is given
concentration leads to	in
a) error in concentration	a) architectural design
b) error in variation	b) logic design
c) error in doping	c) system design
d) distribution error	A) functional design
4 is used to deal with effect of variation.	
a) chip level technique	
b) logic level technique	1,713
c) switch level technique	Mark
A) system level technique	Valle,
5. As die size shrinks, the complexity of	Signature
making the photomasks	
a) increases	and the same of th
b) decreases	COLUMN TO THE REAL PROPERTY.
c) remains the same	Department 188
d) cannot be determined	(2) - 2/- / =
6 architecture is used to design VLSI.	TECE S
a) system on a device	Suducherry
b) single open circuit	
e) system on a chip	PAPAKA
B.Tech. (Mech.), W.I.	ech.(Energy), Ph.D. (IIT Madras) S.T.E., F.I.I.P.E., M.C.S.I M.C.I.I., RINCIPAL
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